Amendments to the Claims:

Claims 1-35 are pending. This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (cancelled)

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (cancelled)

7. (cancelled)

8. (currently amended) A method of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of the partitions comprises the processing unit of at least one of the processors, and where L is an integer ≥ 2 and R is an integer ≥ 1, the method comprising:

connecting the L switches of the L processors among the external ports of the L switches in an extended torus architecture; and

setting the connected L switches thereby interconnecting each of the partitions as a torus, wherein the setting comprises computing the span of the partition, wherein the computing comprises

finding the minimum coordinate, MIN, in the partition,

determining the maximum coordinate, MAX, in the partition,

setting the span of the partition to be equal to the set of coordinates i, where MIN ≤ i ≤ MAX, where i is an integer,

~~The method of claim 6 wherein the computing further comprises:~~

if the span of the partition contains exactly two coordinates, where i and i+1 are the two coordinates that belong to the span,

if the span of the partition contains exactly two coordinates, where i and i+1 are the two coordinates that belong to the span,

if i = 1,

connecting the third external port and the second internal port (E3,I2) of the first switch,

connecting the first external port and the first internal port (E1,I1) of the first switch,

connecting the second external port and the second internal port (E2,I2) of the second switch, and

connecting the first external port and the first internal port (E1,I1) of the second switch;

if i = L−1,

connecting the third external port and the first internal port (E3,I1) of the (L-1)th switch,

connecting the fourth external port and the second internal port (E4,I2) of the (L−1)th switch,

connecting the second external port and the first internal port (E2,I1) of the Lth switch, and

connecting the fourth external port and the second internal port (E4,I2) of the Lth switch; and

otherwise, where 2 ≤ i ≤ L−2,

connecting the third external port and the fourth external port (E3,E4) of the (i−1)th switch,

connecting the second external port and the first internal port (E2,I1) of the ith switch,

connecting the third external port and the second internal port (E3,I2) of the ith switch,

connecting the first external port and the first internal port (E1,I1) of the (i+1)th switch, and

connecting the second external port and the second internal port (E2,I2) of the (i+1)th switch.

9. (currently amended) A method of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of the partitions comprises the processing unit of at least one of the processors, and where L is an integer ≥ 2 and R is an integer ≥ 1, the method comprising:

connecting the L switches of the L processors among the external ports of the L switches in an extended torus architecture; and

setting the connected L switches thereby interconnecting each of the partitions as a torus, wherein the setting comprises computing the span of the partition, wherein the computing comprises

finding the minimum coordinate, MIN, in the partition,

determining the maximum coordinate, MAX, in the partition,

setting the span of the partition to be equal to the set of coordinates i, where MIN $\leq$ i $\leq$ MAX, where i is an integer,

~~The method of claim 6 wherein the computing further comprises:~~

if the span of the partition contains exactly three coordinates, where i, i+1, and i+2 are the three coordinates that belong to the span,

connecting the third external port and the first internal port (E3,I1) of the ith switch,

connecting the fourth external port and the second internal port (E4,I2) of the ith switch,

connecting the first external port and the first internal port (E1,I1) of the (i+2)th switch,

connecting the second external port and the second internal port (E2,I2) of the (i+2)th switch;

if (i+1) belongs to the partition,

connecting the second external port and the first internal port (E2,I1) of the (i+1)th switch and

connecting the third external port and the second internal port (E3,I2) of the (i+1)th switch; and

if (i+1) does not belong to the partition,

connecting the second external port and the third external port (E2,E3) of the (i+1)th switch.

10. (currently amended) A method of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of the partitions comprises the processing unit of at least one of the processors, and where L is an integer ≥ 2 and R is an integer ≥ 1, the method comprising:

connecting the L switches of the L processors among the external ports of the L switches in an extended torus architecture; and

setting the connected L switches thereby interconnecting each of the partitions as a torus, wherein the setting comprises computing the span of the partition, wherein the computing comprises

finding the minimum coordinate, MIN, in the partition,

determining the maximum coordinate, MAX, in the partition,

setting the span of the partition to be equal to the set of coordinates i, where MIN ≤ i ≤ MAX, where i is an integer,

~~The method of claim 6 wherein the computing further comprises:~~

if the span of the partition contains at least four coordinates, for each coordinate i such that MIN ≤ i ≤ MAX,

if i = MIN,

connecting the third external port and the first internal port (E3,I1) of the ith switch and

connecting the fourth external port and the second internal port (E4,I2) of the ith switch;

if i = MAX,

connecting the first external port and the first internal port (E1,I1) of the ith switch and

connecting the second external port and the second internal port (E2,I2) of the ith switch;

if i = MIN + 1 and i belongs to the partition,

connecting the second external port and the first internal port (E2,I1) of the ith switch and

connecting the fourth external port and the second internal port (E4,I2) of the ith switch;

if i = MIN + 1 and i does not belong to the partition,

connecting the second external port and the fourth external port (E2,E4) of the ith switch;

if i = MAX − 1 and i belongs to the partition,

connecting the first external port and the first internal port (E1,I1) of the ith switch and

connecting the third external port and the second internal port (E3,I2) of the ith switch;

if i = MAX − 1 and i does not belong to the partition,

connecting the first external port and the third external port (E1,E3) of the ith switch;

if MIN + 2 ≤ i ≤ MAX − 2 and i belongs to the partition,

connecting the first external port and the first internal port (E1,I1) of the ith switch and

connecting the fourth external port and the second internal port (E4,I2) of the ith switch; and

if MIN + 2 ≤ i ≤ MAX − 2 and i does not belong to the partition,

connecting the first external port and the fourth external port (E1,E4) of the ith switch.

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (cancelled)

15. (cancelled)

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (cancelled)

24. (currently amended) A system of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of the partitions comprises the processing unit of at least one of the processors, and where L is an integer ≥ 2 and R is an integer ≥ 1, the system comprising:

a connecting module configured to connect the L switches of the L processors among the external ports of the L switches in an extended torus architecture; and

a setting module configured to set the connected L switches thereby interconnecting each of the partitions as a torus, wherein the setting module comprises computing module configured to compute the span of the partition, wherein the computing module comprises

a finding module configured to find the minimum coordinate, MIN, in the partition,

a determining module configured to determine the maximum coordinate, MAX, in the partition,

a setting module configured to set the span of the partition to be equal to the set of coordinates i, where $MIN \leq i \leq MAX$, where i is an integer,

~~The system of claim 22 wherein the computing module further comprises:~~

if the span of the partition contains exactly two coordinates, where i and i+1 are the two coordinates that belong to the span,

if i = 1,

a first connecting module configured to connect the third external port and the second internal port (E3,I2) of the first switch,

a second connecting module configured to connect the first external port and the first internal port (E1,I1) of the first switch,

a third connecting module configured to connect the second external port and the second internal port (E2,I2) of the second switch, and

a fourth connecting module configured to connect the first external port and the first internal port (E1,I1) of the second switch;

if i = L−1,

a first connecting module configured to connect the third external port and the first internal port (E3,I1) of the (L-1)th switch,

a second connecting module configured to connect the fourth external port and the second internal port (E4,I2) of the (L−1)th switch,

a third connecting module configured to connect the second external port and the first internal port (E2,I1) of the Lth switch, and

a fourth connecting module configured to connect the fourth external port and the second internal port (E4,I2) of the Lth switch; and

otherwise, where $2 \leq i \leq L-2$,

a first connecting module configured to connect the third external port and the fourth external port (E3,E4) of the (i−1)th switch,

a second connecting module configured to connect the second external port and the first internal port (E2,I1) of the ith switch,

a third connecting module configured to connect the third external port and the second internal port (E3,I2) of the ith switch,

a fourth connecting module configured to connect the first external port and the first internal port (E1,I1) of the (i+1)th switch, and

a fifth connecting module configured to connect the second external port and the second internal port (E2,I2) of the (i+1)th switch.

25. (currently amended) A system of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of

the partitions comprises the processing unit of at least one of the processors, and where L is an integer ≥ 2 and R is an integer ≥ 1, the system comprising:

a connecting module configured to connect the L switches of the L processors among the external ports of the L switches in an extended torus architecture; and

a setting module configured to set the connected L switches thereby interconnecting each of the partitions as a torus, wherein the setting module comprises computing module configured to compute the span of the partition, wherein the computing module comprises

a finding module configured to find the minimum coordinate, MIN, in the partition,

a determining module configured to determine the maximum coordinate, MAX, in the partition,

a setting module configured to set the span of the partition to be equal to the set of coordinates i, where MIN ≤ i ≤ MAX, where i is an integer,

~~The system of claim 22 wherein the computing module further comprises:~~

if the span of the partition contains exactly three coordinates, where i, i+1, and i+2 are the three coordinates that belong to the span,

a first connecting module configured to connect the third external port and the first internal port (E3,I1) of the ith switch,

a second connecting module configured to connect the fourth external port and the second internal port (E4,I2) of the ith switch,

a third connecting module configured to connect the first external port and the first internal port (E1,I1) of the (i+2)th switch,

a fourth connecting module configured to connect the second external port and the second internal port (E2,I2) of the (i+2)th switch;

if (i+1) belongs to the partition,

a fifth connecting module configured to connect the second external port and the first internal port (E2,I1) of the (i+1)th switch and

a sixth connecting module configured to connect the third external port and the second internal port (E3,I2) of the (i+1)th switch; and

if (i+1) does not belong to the partition,

a fifth connecting module configured to connect the second external port and the third external port (E2,E3) of the (i+1)th switch.

26. (currently amended) A system of interconnecting L processors of a parallel computer to facilitate torus partitioning, where each of the processors comprises a processing unit and a switch, where the switch comprises a first external port, a second external port, a third external port, a fourth external port, a first internal port, and a second internal port, where the L processors comprise R non-overlapping partitions, where each of the partitions comprises the processing unit of at least one of the processors, and where L is an integer ≥ 2 and R is an integer ≥ 1, the system comprising:

a connecting module configured to connect the L switches of the L processors among the external ports of the L switches in an extended torus architecture; and

a setting module configured to set the connected L switches thereby interconnecting each of the partitions as a torus, wherein the setting module comprises computing module configured to compute the span of the partition, wherein the computing module comprises

a finding module configured to find the minimum coordinate, MIN, in the partition,

a determining module configured to determine the maximum coordinate, MAX, in the partition,

a setting module configured to set the span of the partition to be equal to the set of coordinates i, where $MIN \leq i \leq MAX$, where i is an integer,

~~The system of claim 22 wherein the computing module further comprises:~~

if the span of the partition contains at least four coordinates, for each coordinate i such that $MIN \leq i \leq MAX$,

if i = MIN,

a first connecting module configured to connect the third external port and the first internal port (E3,I1) of the ith switch and

a second connecting module configured to connect the fourth external port and the second internal port (E4,I2) of the ith switch;

if i = MAX,

a first connecting module configured to connect the first external port and the first internal port (E1,I1) of the ith switch and

a second connecting module configured to connect the second external port and the second internal port (E2,I2) of the ith switch;

if i = MIN + 1 and i belongs to the partition,

a first connecting module configured to connect the second external port and the first internal port (E2,I1) of the ith switch and

a second connecting module configured to connect the fourth external port and the second internal port (E4,I2) of the ith switch;

if i = MIN + 1 and i does not belong to the partition,

a connecting module configured to connect the second external port and the fourth external port (E2,E4) of the ith switch;

if i = MAX − 1 and i belongs to the partition,

a first connecting module configured to connect the first external port and the first internal port (E1,I1) of the ith switch and

a second connecting module configured to connect the third external port and the second internal port (E3,I2) of the ith switch;

if i = MAX − 1 and i does not belong to the partition,

a connecting module configured to connect the first external port and the third external port (E1,E3) of the ith switch;

if MIN + 2 ≤ i ≤ MAX − 2 and i belongs to the partition,

a first connecting module configured to connect the first external port and the first internal port (E1,I1) of the ith switch and

a second connecting module configured to connect the fourth external port and the second internal port (E4,I2) of the ith switch; and

if MIN + 2 ≤ i ≤ MAX − 2 and i does not belong to the partition,

a connecting module configured to connect the first external port and the fourth external port (E1,E4) of the ith switch.

27. (cancelled)

28. (cancelled)

29. (cancelled)

30. (cancelled)

31. (cancelled)

32. (cancelled)

33. (cancelled)

34. (cancelled)

35. (cancelled)